CLAIMS

What is claimed is:

1. A content addressable memory (CAM) device comprising:

a CAM array;

an error detection circuit coupled to receive a data value from a selected storage location within the CAM array, the error detection circuit being adapted to generate an error indication according to whether the data value includes an error; and

an error storage circuit coupled to receive the error indication from the error detection circuit, the error storage circuit being adapted to store an error address that corresponds to the selected storage location if the error indication indicates that the data value includes an error and if the error address is not already stored within the error storage circuit.

2. The content addressable memory device of claim 1 wherein the error detection circuit includes a parity checking circuit to generate a first parity bit based on the data value and to compare the first parity bit with a parity bit within the data value.

3. The content addressable memory device of claim 2 wherein the parity checking circuit is adapted to generate the error indication according to whether the first parity bit matches the parity bit within the data value.

4. The content addressable memory device of claim 1 wherein the error storage circuit comprises:

a storage array having a plurality of error address storage locations; and

compare circuitry to compare the error address with contents of the plurality of error address storage locations and to generate a match indication according to whether the error address matches the content of any of the plurality of error address storage locations.

5. The content addressable memory device of claim 4 wherein the compare circuitry comprises a plurality of compare circuits coupled to the plurality of error address storage locations, each of the compare circuits being adapted to compare the error address with contents of a corresponding one of the plurality of error address storage locations.

6. The content addressable memory device of claim 5 wherein each of the compare circuits is coupled to a respective one of a plurality of match lines, and wherein each of the compare circuits is further adapted to affect a level of the respective one of the plurality of match lines according to whether the error address matches the content of the corresponding one of the plurality of error address storage locations.

7. The content addressable memory device of claim 4 wherein the error storage circuit further comprises a control circuit coupled to the error detection circuit, the storage array and the compare circuitry, the control circuit being responsive to the match indication from the compare circuitry and the error indication from the error detection circuit to selectively store the error address in the storage array.

8. The content addressable memory device of claim 7 wherein the control circuit is adapted to store the error address in the storage array if the error indication generated by the error detection circuit indicates that the data value includes an error and if the match indication

generated by the compare circuitry indicates that the error address is not already stored within the storage array.

9. An apparatus comprising:

a first content addressable memory (CAM) array having storage rows and compare circuitry to generate match signals that indicate whether a comparand value matches contents of one or more of the storage rows;

a priority encoder coupled to receive the match signals from the first CAM array and having circuitry to output, in response to the match signals, a match address that corresponds to one of the storage rows; and

error circuitry coupled to the first CAM array and to the priority encoder, the error circuitry being adapted to determine whether any of the storage rows includes corrupted content and, for each storage row determined to include corrupted content, to store an error address that corresponds to the storage row if the error address is not already stored in the error circuitry, the error circuitry being further adapted to compare the match address to each error address stored by the error circuitry.

10. The apparatus of claim 9 wherein the error circuitry is further adapted to assert a match error signal if the match address matches an error address stored by the error circuitry.

11. The apparatus of claim 9 wherein the error circuitry comprises:

an error detection circuit coupled to receive contents of the storage rows of the first CAM array and adapted to determine whether the contents of the storage rows include corrupted content and to assert an error signal for each of the storage rows determined to include corrupted content; and

a second CAM array coupled to receive the error signal from the error detection circuit and adapted to store a respective error address for each of the storage rows for which the error signal is asserted if the error address is not already stored in the second CAM array.

12. The apparatus of claim 11 wherein the second CAM array comprises a first comparand port to compare one or more error addresses stored in the CAM array with an error address that corresponds to a storage row for which the error signal is asserted.

13. The apparatus of claim 12 wherein the second CAM array comprises a second comparand port to compare the match address with the one or more error addresses stored in the CAM array.

14. The apparatus of claim 13 wherein the second CAM array further comprises a plurality of CAM cells, each of the CAM cells including a first compare circuit coupled to the first comparand port and a second compare circuit coupled to the second comparand port.

15. The apparatus of claim 14 wherein the plurality of CAM cells are organized in rows, the second CAM array further comprising a first plurality of match signal lines and a second plurality of match signal lines, each match signal line of the first plurality of match signal lines being coupled to the first compare circuit within each CAM cell of a respective row of the plurality of CAM cells, and each match signal line of the second plurality of match signal lines being coupled to the second compare circuit within each CAM cell of a respective row of the plurality of CAM cells.

16. The apparatus of claim 15 wherein the second CAM array comprises:

a first match logic circuit coupled to the first plurality of match signal lines; and

a second match logic circuit coupled to the second plurality of match signal lines.

17. The apparatus of claim 16 wherein the second match logic circuit is adapted to generate a match error signal if any of the second plurality of match signal lines indicates a match between an error address stored in the corresponding row of CAM cells and the match address.

18. The apparatus of claim 16 wherein the first match logic circuit is adapted to prevent storage of an error address in the CAM array if any of the first plurality of match signal lines indicates a match between the error address and an error address stored in the corresponding row of CAM cells.

19. The apparatus of claim 11 further comprising a select circuit having a first input coupled to receive the match address from the priority encoder, a second input coupled to receive an error address that corresponds to a storage row for which the error signal is asserted, and an output coupled to a comparand port of the second CAM array.

20. The apparatus of claim 19 wherein the select circuit is responsive to a select signal to select either the match address or the error address to be output to the comparand port of the second CAM array.

21. A method of operation within a content addressable memory (CAM) device, the method comprising:

determining that a first data value stored in a first storage array of the CAM device includes an error;

determining whether the storage address of the first data value matches one or more storage addresses stored in a second storage array of the CAM device; and

storing the storage address of the first data value in the second storage array if the storage address of the first data value does not match the one or more storage addresses stored in the second storage array.

22. The method of claim 21 wherein determining that a first data value stored in a first storage array of the CAM device includes an error comprises determining that the data value includes a parity error.

23. The method of claim 21 wherein determining whether the storage address of the first data value matches one or more storage addresses stored in a second storage array of the CAM device comprises comparing the storage address of the first data value with each of the one or more storage addresses stored in the second storage array.

24. The method of claim 23 wherein comparing the storage address of the first data value with each of the one or more storage addresses stored in the second storage array comprises simultaneously comparing the storage address of the first data value with each of the one or more storage addresses stored in the second storage array.

25. The method of claim 21 further comprising:

determining a storage address of a second data value within the first storage array;

comparing the storage address of the second data value with each of the one or more storage addresses stored in the second storage array; and

asserting an error signal if the storage address of the second data value matches any of the

one or more storage addresses stored in the second storage array.

26. The method of claim 25 wherein comparing the storage address of the second data value with each of the one or more storage addresses stored in the second storage array comprises simultaneously comparing the storage address of the second data value with each of the one or more storage addresses stored in the second storage array.

27. The method of claim 25 wherein comparing the storage address of the second data value with each of the one or more storage addresses stored in the second storage array comprises comparing the storage address of the second data value with each of the one or more storage addresses stored in the second storage array concurrently with comparing the storage address of the first data value with each of the one or more storage addresses stored in the second storage array.

28. The method of claim 25 wherein determining a storage address of a second data value within the first storage array comprises comparing a comparand value to each of a plurality of data values stored in the first storage array to identify the second data, the second data value being one of the plurality of values that matches the comparand value.

29. The method of claim 25 further comprising selecting, according to a select signal, either the first data value or the second data value to be compared with the one or more storage addresses stored in the second storage array.

30. The method of claim 21 wherein the first storage array comprises a first array of CAM cells and wherein the second storage array comprises a second array of CAM cells.

31. A content addressable memory (CAM) device comprising:

a first storage array to store data values;

a second storage array to store storage addresses;

means for determining that a first data value stored in the first storage array includes an error;

means for determining whether the storage address of the first data value matches one or more storage addresses stored in the second storage array; and

means for storing the storage address of the first data value in the second storage array if the storage address of the first data value does not match the one or more storage addresses stored in the second storage array.

32. The CAM device of claim 31 wherein the means for determining whether the storage address of the first data value matches one or more storage addresses stored in the second storage array comprises means for comparing the storage address of the first data value with each of the one or more storage addresses stored in the second storage array.